In the Claims

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A reconfigurable processor integrated circuit, comprising:

a processor core for operating on a set of instructions to carry out predefined processes;

a plurality of input/output pins;

a plurality of functional input/output blocks each having an input and an output and associated with said processing core to allow said processing core to interface with said plurality of input/output pins, each of said functional input/output blocks having an associated and predetermined functionality, said functionality being the output as a function of the input, the function defined by said functionality, and each of said functional input/output blocks having a requirement for a defined number of said plurality of input/output pins wherein the total of said defined number for all of said plurality of functional input/output blocks exceeds the number of said plurality of input/output pins, wherein said processor core is interfaced with one of said input or output of each of said functional blocks;

a reconfigurable interface for selectively interfacing between the other of said input or output of said functional blocks and a select one or ones of said plurality of input/output pins, such that said processor core can be interfaced with said select one or ones of said input/output pins, said reconfigurable interface operable to define how each of said plurality of input/output pins interfaces with said select ones of said plurality of functional blocks and the associated functionality in accordance with configuration information; and

a non-volatile memory for storing said configuration information, such that said stored configuration information can be altered.

Claim 2 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1, wherein said plurality of input/output pins are configured in functional groups.

Claim 3 (Previously presented): The reconfigurable processor integrated circuit of Claim 1, wherein said each of said functional input/output blocks has a plurality of inputs and outputs and each of said plurality of said input/output pins can be interfaced with any of said plurality of functional input/output blocks by said reconfigurable interface.

Claim 4 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1, wherein said reconfigurable interface is programmable by said user.

Claim 5 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1, wherein said processor core is a digital processor core and further comprising an analog section for interfacing via input/output analog pins with analog signals and for interfacing with said processor core with a digital interface.

Claim 6 (Previously Presented): The reconfigurable processor integrated circuit of Claim 5, wherein said input/output analog pins are not reconfigurable with said reconfigurable interface.

Claims 7-13 (Canceled)

Claim 14. (Previously Presented): The integrated circuit of Claim 1, wherein each of said functional input/output blocks has a predetermined functionality associated therewith that is modifiable to modify the associated function.

Claim 15: (Previously Presented) The integrated circuit of Claim 14, wherein said processor core is operable to input to a select one of said functional input/output blocks on the associated input thereof control information to modify the function associated therewith.

Claim 16: (Previously Presented) The integrated circuit of Claim 14, wherein said processor core is operable during normal operation of the integrated circuit to modify the function of one or more of said functional input/output blocks.

Claim 17: (Previously Presented) The integrated circuit of Claim 1, wherein the one of the inputs and outputs of each of said functional blocks interfaced with said processor core has a special function register associated therewith, such that any signals received from said processor core are stored therein and any signals transmitted to said processor core from the associated one of said functional input/output blocks is stored therein.

Claim 18: (Previously Presented) The integrated circuit of Claim 17, and further comprising a special function register bu for interfacing between said processor core and said special function registers, wherein each of said special function registers has an address associated therewith that is

within an address space of said processor core.